R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

Applicant thanks Examiner Psitos for the indications of allowable matter.

SUPPORT FOR THE DRAWING AMENDMENTS

Support for the new drawing may be found in the specification, for example, on page 24 lines 4-15 as originally filed. Thus, no new matter has been added.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and new claims may be found in the specification, for example, on page 11 line 13 thru page 12 line 6, page 12 lines 13-16, page 23 lines 7-9, page 24 lines 4-9, FIGS. 1, 2, 5 and 10 and claims 1, 6, 12 and 13, as originally filed. Thus, no new matter has been added.

PRIORITY UNDER 35 U.S.C. §119

The Examiner is respectfully requested to acknowledge the claim for foreign priority under 35 U.S.C. §119 to United Kingdom Application No. 0026105.7, filed October 25, 2000.

CLAIM OBJECTION

The objection to claim 10 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 10 under 35 U.S.C. §112, first paragraph, has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 4, 5 and 9 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-4 and 10 under 35 U.S.C. §102(e) as being anticipated by Eom '830 is respectfully traversed and should be withdrawn.

The rejection of claims 1-3 under 35 U.S.C. §102(e) as being unpatentable over Katoh '311 has been obviated by appropriate amendment and should be withdrawn.

Eom concerns an apparatus and method for detecting wobble defect (Title). Katoh concerns an optical disc device (Title). In contrast, the present invention has a priority date of October 25, 2000 that predates Eom. Therefore, Eom is not a valid 35 U.S.C.

§102(e) reference. As such, the rejection of claims 1-4 and 10 based on Eom should be withdrawn.

Claim 1 provides (in part) a step for timing a duration for each of a plurality of first periods for an intermittent clock signal. In contrast, Katoh appears to be silent regarding any timing process that times a duration of an intermittent clock signal when the intermittent clock signal is present. Therefore, Katoh does not appear to disclose or suggest a step for timing a duration for each of a plurality of first periods for an intermittent clock signal as presently claimed.

Claim 1 further provides a step for holding a phase lock loop in a free-running state during a plurality of second periods when an intermittent clock signal is absent in response to a duration indicating an end to one of a plurality of first periods. In contrast, Katoh appears to be silent regarding any process for holding a phase lock loop in a free-running state when an intermittent clock signal is absent in response to a duration indicating an end to a first period. Therefore, Katoh does not appear to disclose or suggest a step for holding a phase lock loop in a free-running state during a plurality of second periods when an intermittent clock signal is absent in response to a duration indicating an end to one of a plurality of first periods as presently claimed.

Furthermore, the assertion on page 5 of the Office Action that figures 2, 6 and 8 of Katoh illustrate a PLL in a free running state appears to be incorrect. The text in column 8, line 50 thru column 9, line 37 of Katoh indicates that a channel PLL 1 is in an acquisition state during header 26 as indicated by the rising control voltage (V0 to V1). Katoh appears to be silent regarding a wobble PLL 20 operating in a free-running state during a plurality of periods when an intermittent clock signal is absent. Therefore, none of the PLLs discussed by Katoh appear to have a free-running state during a plurality of second periods when an intermittent clock signal is absent in response to a duration indicating an end to one of a plurality of first periods as presently claimed. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-5 and 10 under 35 U.S.C. §103(a) as being unpatentable over Eom in view of Katoh is respectfully traversed and should be withdrawn.

The rejection of claims 1-4, 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over Eom in view of Shim '902 is respectfully traversed and should be withdrawn.

The rejection of claims 4 and 5 under 35 U.S.C. §103(a) as being unpatentable over Katoh in view of Shim has been obviated in part by appropriate amendment, is respectfully traversed in part and should be withdrawn.

The rejection of claims 4 and 5 under 35 U.S.C. §103(a) as being unpatentable over Katoh in view of Minamino et al. '929 (hereafter Minamino) has been obviated in part by appropriate amendment, is respectfully traversed in part and should be withdrawn.

Eom concerns an apparatus and method for detecting wobble defect (Title). Katoh concerns an optical disc device (Title). Shim concerns a method for generating land/groove switching signal from POLG type disc and apparatus therefore (Title). Minamino concerns an optical disk recording apparatus and method for recording data on optical disk (Title). In contrast, the present invention has a priority date of October 25, 2000 that predates Eom. Therefore, Eom is not a valid 35 U.S.C. §103(a) reference. As such, the rejections of claims 1-5, 10 and 11 based on Eom should be withdrawn.

Claim 4 provides a step for placing a phase lock loop in the free-running state in advance of reading a header region on an optical disk in response to a duration of a plurality of first periods of a intermittent clock signal when the intermittent clock signal is present. In contrast, each of Katoh and Minamino appear

to be silent regarding any processing knowing in advance when an intermittent clock signal is about to disappear. In particular, the "window" illustrated in FIGS. 2 and 3 of Minamino (asserted similar to the claimed duration) appear to exist at an **end** of an ID section (header region), not in **advance** of the ID section. Therefore, Katoh and Minamino, alone or in combination, do not appear to teach or suggest a step for placing a phase lock loop in the free-running state in advance of reading a header region on an optical disk in response to a duration of a plurality of first periods of a intermittent clock signal when the intermittent clock signal is present as presently claimed.

Furthermore, Shim appears to be silent regarding a window signal "HDWIN" (asserted similar to the claimed duration) being used to control a mode or state of a PLL. In particular, the signal HDWIN only appears to be used in generation of signals HDBT and HDPK as discussed in column 10, lines 38-44 of Shim. Thus, no evidence for (i) motivation to combine or (ii) a reasonable expectation of success appears to exist to use the signal HDWIN from Shim to control a PLL from Katoh as suggested on page 6 of the Office Action. Therefore, *prima facie* obviousness has not been established per MPEP §2142. As such, claim 4 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 5 provides a step for seeking to acquire phase lock only after re-emergence of an intermittent clock signal has been

validated. Despite the assertion on page 6 of the Office Action, FIG. 6 of Katoh appears to show the channel PLL 1 in an acquisition phase during header 26 due to changes in the control voltage during the header 26 period as discussed in column 8, line 50 thru column 9, line 37 of Katoh. Katoh appears to contemplate seeking phase lock **during and after** the header 26, not **only after** validation as presently claimed. The rest of Katoh appears to show phase lock acquisition **during** each header period prior to achieving a phase lock. Shim and Minamino do not appear to cure the defect in Katoh. Therefore, Katoh, Shim and Minamino, alone or in combination, do not appear to teach or suggest a step for seeking to acquire phase lock only after re-emergence of an intermittent clock signal has been validated as presently claimed. As such, claim 5 is fully patentable over the cited references and the rejection should be withdrawn.

The perceived allowable matter of claims 6, 9, 12 and 13 have been rewritten into independent form. Therefore, claims 6-9, 12-15 and 20-28 should be allowed. As such, the presently claimed invention is fully patentable over the cited references and the objections should be withdrawn.

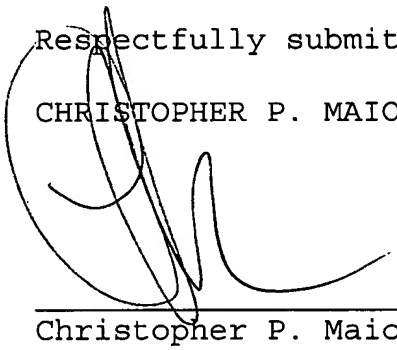
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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